Beyond carbon nanotube thin-film transistors: Logic circuits, memory, and heterostructures

Mark C. Hersam
Department of Materials Science and Engineering, Northwestern University
Contact e-mail: *m-hersam@northwestern.edu*

With the availability of large quantities of electronically monodisperse carbon nanotubes (CNTs), homogeneous semiconducting CNT thin films can be produced through a variety of solution-based methods including vacuum filtration, dielectrophoresis, evaporation-driven self-assembly, aerosol jet printing, and inkjet printing. Through careful integration of these thin films with high-k gate dielectrics, CNT thin-film transistors (TFTs) can achieve device metrics that are competitive with polycrystalline silicon and amorphous oxide semiconductors. Furthermore, with appropriate device geometries, doping schemes, and gate electrode materials, threshold voltage can be tuned to enable enhancement-mode p-type and n-type TFTs, resulting in CNT CMOS logic gates with subnanowatt static power dissipation and full rail-to-rail voltage swing. While these results suggest that very-large-scale integration (VLSI) should be possible for CNT thin-film circuits, further improvements are needed in CNT TFT large-area spatial homogeneity and long-term environmental stability. Towards these ends, this talk will introduce encapsulation schemes and automated measurement strategies that yield wafer-scale CNT TFT arrays with sufficiently tight control over on/off ratio, subthreshold swing, and threshold voltage for VLSI CNT thin-film circuits. Using this methodology, large-area arrays of fully functional CNT TFT static random access memory (SRAM) cells are demonstrated with desirable static noise and write margins.